IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
SHERMAN DIVISION

STMICROELECTRONICS, INC.	§	
	§	
Plaintiff	§	
	§	
vs.	§	
	§	
MOTOROLA, INC.	§	
	§	**CASE NO. 4:03-CV-276**
Defendant,	§	
Counterclaim Plaintiff	§	
	§	
vs.	§	
	§	
STMICROELECTRONICS, N.V., AND STMICROELECTRONICS, INC.	§	
	§	
Counterclaim Defendants	§	

MEMORANDUM OPINION AND ORDER

The Court withdraws its Memorandum Opinion and Order of July 13, 2004 (Docket No. 168) and substitutes this Opinion in its place. Before the Court are seven patents with terms to be construed. STMicroelectronics, N.V. ("ST") has asserted three patents: U.S. Patent No. 5,812,789 (the "`789" or "Diaz" patent); U.S. Patent No. 5,031,092 (the "`092" or "Edwards" patent); and U.S. Patent No. 5,359,244 (the "`244" or "Hopkins" patent). Motorola, Inc. ("Motorola") has asserted four patents: U.S. Patent No. 5,155,563 (the "`563" or "Davies" patent); U.S. Patent No. 4,548,654 (the "`654" or "Tobin" patent); U.S. Patent No. 5,776,798 (the "`798" or "Quan" patent); and U.S. Patent No. 5,084,814 (the "`814" or "Vaglica" patent). Having considered the parties' submissions

and oral argument, the Court construes the disputed terms as follows in this Opinion.[1]

LAW OF CLAIM CONSTRUCTION

In claim construction, courts examine the patent's intrinsic evidence to define the patented invention's scope. *Bell Atlantic Network Servs., Inc. v. Covad Communications Group, Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). First, courts give "claim terms their ordinary and accustomed meaning as understood by one of ordinary skill in the art." *Alloc, Inc. v. Int'l Trade Commission*, 342 F.3d 1361, 1368 (Fed. Cir. 2003); *Id.* Second, the court must determine whether it must deviate from the claim language's ordinary and accustomed meaning. *Bell Atlantic Network Servs., Inc.*, 262 F.3d at 1268. There is a "heavy presumption" that claim terms carry their ordinary and customary meaning which is only rebutted if the patent "expresses an intention to impart novel meaning to [them]." *Sunrace Roots Enter. Co., LTD v. SRAM Corp.*, 336 F.3d 1298, 1302 (Fed. Cir. 2003); *Id.* "This presumption is overcome: (1) where the patentee has chosen to be his own lexicographer, or (2) where a claim term deprives the claim of clarity such that there is no means by which the scope of the claim may be ascertained from the language used." *Bell Atlantic Network Servs., Inc.*, 262 F.3d at 1268. When a court attempts to define a term, it "immerses itself in the specification, the prior art, and other evidence, such as the understanding of skilled artisans at the time of the invention, to discern the context and normal usage of the words in the patent claim." *Alloc, Inc.*, 342 F.3d at 1368.

The Federal Circuit has held that "among the intrinsic evidence, the specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide

[1]For ease of reference, the Court has attached a Claim Construction Chart as Appendix A to this Opinion. The Claim Construction Chart contains the Court's construction of agreed and disputed terms.

to the meaning of a disputed term." *Teleflex, Inc. v. Ficosa North America Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002). This is true because a patentee may define his own terms. Also, the specification may resolve ambiguous claim terms "where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone." *Id*. However, the specification may not redefine particular claim terms away from their ordinary meaning unless the intrinsic evidence "clearly set[s] forth or clearly redefine[s] a claim term so as to put one reasonably skilled in the art on notice that the patentee intended to so redefine the claim term." *Bell Atlantic Network Servs., Inc.*, 262 F.3d at 1268 (internal quotations omitted). Thus, "although the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims." *Comark Communications, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998).

The patents in suit also contain means-plus-function limitations that require construction. Where a claim limitation is expressed in "means plus function" language and does not recite definite structure in support of its function, the limitation is subject to 35 U.S.C. § 112, ¶ 6. *Braun Medical, Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997). In relevant part, 35 U.S.C. § 112, ¶ 6 mandates that "such a claim limitation 'be construed to cover the corresponding structure . . . described in the specification and equivalents thereof.'" *Id*. (citing 35 U.S.C. § 112, ¶ 6). Accordingly, when faced with means-plus-function limitations, courts "must turn to the written description of the patent to find the structure that corresponds to the means recited in the [limitations]." *Id*.

Construing a means-plus-function limitation involves multiple inquiries. "The first step in

construing [a means-plus-function] limitation is a determination of the function of the means-plus-function limitation." *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001). Once a court has determined the limitation's function, "the next step is to determine the corresponding structure disclosed in the specification and equivalents thereof." *Id*. A "structure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Id*. Moreover, the focus of the "corresponding structure" inquiry is not merely whether a structure is capable of performing the recited function, but rather whether the corresponding structure is "clearly linked or associated with the [recited] function." *Id*.

THE `789 DIAZ PATENT

The Diaz patent involves encoding and decoding signals in electronic devices. An encoder is a device that takes a video or audio signal and compresses the signal to a reduced size using an encoding standard. For example, a video camera takes a video signal and compresses it for storage on a tape, disk, or flash card. A decoder is a device that decompresses the compressed signal for use. For example, a DVD player decompresses recorded video from a DVD so that one may view the video.

The Diaz patent describes technology that allows an encoder or decoder to share memory with other devices on the same electronic system. Decoding and encoding audio and video without any loss of data or other interruption can require significant amounts of memory. Before the Diaz patent, electronic systems would often incorporate dedicated memory that serviced only the encoder or decoder. Although the dedicated memory allowed for efficient operation, it also increased the device's cost. The Diaz patent allows an encoder or decoder to operate without interruption and

without expensive dedicated memory. The Diaz patent discloses a shared memory interface with an arbiter device that regulates the memory access from the decoder/encoder and other devices to the shared memory.

Real Time Operation

The Court adopts ST's proposed construction of "real time operation" and construes it to mean "processing fast enough to keep up with an input data stream." In part, the Court finds that a person of ordinary skill in the art would apply ST's proposed construction as the term's ordinary meaning because the relevant technical dictionary defines "real time" as "a system or mode of operation in which computation is performed during the actual time that an external process occurs." *IEEE Standard Dictionary of Elec. & Elecs. Terms*, at 879 (6th ed. 1996). The relevant dictionary definition indicates that real time concerns the processor's ability to "keep up with" the data input. Moreover, because the term is concerned with the processor's ability to keep up with the input, Motorola's proposed construction[2] improperly shifts the focus to the viewer or listener.

Selectively Providing Access

The Court adopts ST's proposed construction of "selectively providing access" and construes it to mean "determining which of a plurality of devices coupled to a bus is allowed access to the memory based on a priority scheme." Comparison of ST's proposed construction with Motorola's[3] demonstrates agreement that the term should include: multiple devices, a bus, memory access, and a priority scheme. The dispute over this term regards Motorola's attempt to include other limitations

[2]Motorola's proposed construction is: "operation of the decoder so that the rate of decoding is faster or the same as the display rate and the human viewer or listener cannot detect any loss of information."

[3]Motorola's proposed construction is: "providing access using a priority scheme that ensures that the decoder operates in real time, without denying the other components on the bus access to the memory for an amount of time that would interfere with their operation."

in this claim term. For example, Motorola would include the limitation "that the decoder operates in real time" in the definition of "selectively providing access." Although it is true that claim 1 of the Diaz patent concerns real time operation, that limitation is found in the claim language "requires access to the memory sufficient to maintain real time operation." `789 Patent, 12: 31-32. The Court adopts ST's proposed construction as following the ordinary meaning to one skilled in the art and denies Motorola's for incorporating unrelated limitations from the claims and specification.

Sufficient Bandwidth

The Court construes the term "sufficient bandwidth" to mean "sufficient data transfer capability." In this instance, both parties' proposed constructions[4] improperly include limitations found elsewhere in the claims or specification. For example, ST would include the limitation "that allows real time operation" in the term "sufficient bandwidth." However, the "real time" limitation is found elsewhere in the claim and does not need to be repeated in this term. *See* `789 Patent, 12: 31-32. The Court's construction describes the understanding of one skilled in the art without unnecessary limitations.[5]

THE `092 EDWARDS PATENT

The Edwards patent discloses technology that allows for the creation of a single-chip microcomputer with memory. When integrated circuits are connected to peripheral equipment, such as memory necessary to perform computations and instructions, the connections between the processor and peripheral equipment can create bottlenecks that slow performance. The Edwards

[4]ST's proposed construction is: "data transfer capability at a rate that allows for real time operation." Motorola's proposed construction is: "equal to greater than the badwidth required for the decoder to operate in real time without denying the other components on the bus access to memory for an amount of time that would interfere with their operation."

[5]ST agreed to the Court's construction at the *Markman* hearing.

patent purports to solve the bottleneck problem by including the processor and memory circuitry on a single, integrated-circuit chip. Thus, the Edwards patent discloses a complete microcomputer on a single chip.

Additionally, the Edwards patent discloses means of isolating on-chip microcomputer components from one another to solve the problem of interfering electrical signals. The microcomputer components (such as transistors, capacitors, and resistors) are formed in the semiconductor material. When the different circuits on the chip operate, they can produce electrical signals that interfere with one another. The Edwards patent discloses different methods of manipulating the semiconductor material to isolate components from electrical signals produced by other components.

Writable Memory

The Court construes the term "writable memory" to mean "memory that is capable of having data written to and read from." First, for memory to be of any use, it must have the ability to be read from. And thus the "read from" limitation is inherent in the term's construction. Second, the Court declines to accept ST's proposed definition, "a read-write memory," due to Motorola's objection that it is ambiguous. Third, the Court also rejects Motorola's proposed definition[6] because it unnecessarily complicates the definition. Motorola's proposed language requiring "writing information into the cells of the array" is included in other claim language describing the writable memory as "a high density memory array," and thus it is not necessary to include the "array" limitation in the term "writable memory." `092 Patent, 49: 22-24.

Substrate of Semiconductor Material of a First Type

[6]Motorola's proposed construction is: "memory capable of writing information into the cells of the array."

The Court construes the term "substrate of semiconductor material of a first type" as "the base layer of an integrated circuit doped to be either p-type or n-type." Pursuant to the parties' argument at the *Markman* hearing, this construction comports with both parties' proposed constructions.

High Density Memory Array

The Court next addresses the term "high density memory array" in claim 23 of the Edwards patent. ST proposes that the term mean "a memory array having a large number of memory cells for a given area." ST's proposed construction mirrors the plain language of the term and illustrates that none of the four words in this term have a meaning that a person of ordinary skill in the art would not understand. In contrast, Motorola proposes that the Court construe the term to mean: "an array of high density memory cells. 'High Density' memory would have been understood by one of ordinary skill in the art in the early 1980's as including high impedance resistive load SRAM, DRAM, thin film transistors and three-transistor memory cells, but not including depletion transistor loads or complementary pull-up transistors." Whereas ST's proposed construction simply reflects the plain meaning of the term's four words, Motorola's construction requires importing limitations from the specification and speculating on what a person of ordinary skill in the early 1980's would have thought.

The Court adopts ST's proposed construction. First, as noted above, the Court finds that ST's proposed construction mirrors the plain and ordinary meaning of the term's words. *Sunrace Roots Enter. Co., LTD v. SRAM Corp.*, 336 F.3d 1298, 1302 (Fed. Cir. 2003) (finding a "heavy presumption" that claim terms carry their ordinary and customary meaning which is only rebutted if the patent "expresses an intention to impart novel meaning to [them]"). Second, although the

specification does mention the limitations that Motorola would import, the Court finds that those limitations are examples rather than a disclaimer of claim scope. To support its construction, Motorola cites specification language declaring "this *example* uses static RAM cells (SRAM) using high impedance resistive loads rather than the more conventional depletion transistor loads or complimentary pull-up transistors." `092 Patent, 42:50-53 (emphasis added). The Court does not find that this language clearly redefines the term because the patentee clearly described these limitations as an "example." As such, the Court will not import this limitation from the specification. *Bell Atlantic Network Servs., Inc. v. Covad Communications Group, Inc.*, 262 F.3d 1258, 1268 (Fed. Cir. 2001) (holding that the specification may not redefine particular claim terms away from their ordinary meaning unless the intrinsic evidence "clearly set[s] forth or clearly redefine[s] a claim term so as to put one reasonably skilled in the art on notice that the patentee intended to so redefine the claim term"); *Comark Communications, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) ("although the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims."). And third, because the claim language appears to be clear on its face, the Court does not find persuasive Motorola's extraneous evidence regarding how persons of ordinary skill in the art in the early 1980s would have interpreted the term. *See Telelex, Inc. v. Ficosa North America Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002) (holding that the intrinsic evidence is the most significant source of information regarding claim construction).

Circuitry Operable Independently of the Operation of Said Memory Array

The Court adopts ST's proposed construction and construes "circuitry operable independently of the operation of said memory array" as "circuitry whose operation is not contingent upon

operation of the memory array." The Court holds that ST's proposal most clearly represents the meaning as understood by one of ordinary skill in the art. Moreover, the Court declines Motorola's proposed construction[7] for two reasons. First, the proposed limitation "located on the same chip as the memory array" appears redundant of the immediately preceding claim language "a plurality of on-chip transistors comprising." `092 Patent, 50:7-8. Second, Motorola's proposed word "asynchronously" would interject the requirement that the components work in relation to one another. The patent discusses independent operation, and the Court finds no cause to interject asynchronous or synchronous requirements.

Isolation Region in Said Substrate

The Court adopts Motorola's proposed construction of "isolation region in said substrate" and construes that term to mean "region in the substrate isolated from noise generated in another region." ST proposes an identical construction except with the word "area" substituted for "region."[8] The Court finds "region" to be clear on its face and thus denies ST's proposal.

First and Second Regions Noise Isolated from Each Other

The Court adopts Motorola's proposed construction of "first and second regions noise isolated from each other" and construes that term to mean "first and second regions, each region isolated from noise produced in the other region." The Court finds that ST's proposal[9] is improper because contrary to the claim language, it would not require both regions to be noise isolated.

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[7]Motorola's proposed construction is: "circuitry operable asynchronously from the memory array and located on the same chip as the memory array."

[8]ST's proposed construction is: "an area in the substrate isolated from noise generated in another area."

[9]ST's proposed construction is: "first and second areas with one area being isolated from noise produced in the other area."

Noise

The Court adopts ST's proposed construction of "noise" and construes the term as "unwanted electrical signals." The Court finds that ST's construction matches the appropriate dictionary definition and represents the understanding of one skilled in the art. *Webster's New Collegiate Dictionary*, at 772 (1980); *see also Texas Digital Sys., Inc. v. Telegenix, Inc.*, 308 F.3d 1193, 1202 (Fed. Cir. 2002) (holding that dictionaries are reliable sources of information regarding the understanding of those skilled in the art). Although Motorola also derives its proposed construction[10] from a relevant dictionary, the Court rejects Motorola's construction because it introduces an ambiguity. Motorola would have the Court construe "noise" to be only that which "produce[s] undesirable effects," but Motorola does not indicate what constitutes an "undesirable effect."

[Noise] Due to Independent Operation of Said Transistors

The Court adopts ST's proposed construction of "[noise] due to independent operation of said transistors" and construes the term to mean "noise caused by operation of a plurality of on-chip transistors whose operation is not contingent upon operation of the memory array." The Court agrees that the transistors are on-chip and that "independent operation" refers to the relationship between the transistors and memory array. Moreover, the Court rejects Motorola's proposed definition in part because of the term "asynchronous." As discussed *supra*, the Edwards patent discusses independent operation, and the Court finds no cause to interject asynchronous or synchronous requirements that are not mentioned.

THE `244 HOPKINS PATENT

[10]Motorola's proposed construction is: "unwanted electrical signals that produce undesirable effects in the circuits of the control systems in which they occur."

The Hopkins patent describes an efficient method of activating a MOS power transistor. Although one can quickly activate a power transistor by asserting a large charge, once activated, a transistor only requires a small charge to remain active. The Hopkins patent discloses a two gate-drive circuit configuration to reduce power waste. One gate-drive circuit applies a large charge to quickly activate the transistor. Once the transistor is activated, the second gate drive circuit activates in the first circuit's place and applies a smaller charge to maintain the transistor. Thus, the Hopkins method quickly activates a transistor with a large gate-drive circuit, but does not waste energy by unnecessarily running the large circuit.

A First Gate Drive Circuit for Charge Pumping a Node

The Court first addresses the term "a first gate drive circuit for charge pumping a node." ST argues that the term should be construed as "a first circuit that drives a power transistor by alternately taking on charge and delivering charge to the gate of the transistor in a repetitive process." Motorola asserts that the term should be construed as "a first charge pump that delivers charge to the gate of the MOS power transistor by shifting the negative side of a first capacitor from a lower voltage to a higher voltage, wherein said capacitor is not an external capacitor."

The Court declines to accept either proposed construction and instead construes the term to mean "a first circuit that drives a power transistor by raising the electrical potential in an additive, charge transfer process in the manner of a pump." First, the Court does not simply replace the term "gate drive circuit" with "charge pump" because of ambiguities that may be added. Motorola admits that it cannot find a dictionary definition for "charge pump," and the Court is not willing to insert a term having unknown boundaries. Therefore, the Court's construction describes the gate drive circuit's function "in the manner of a pump" without exchanging one ambiguous term for another.

Second, ST's description of "alternately taking on charge and delivering charge to the gate of the transistor in a repetitive process" is also inadequate. The purpose of the first gate drive circuit is to raise the transistor's electrical potential to an appropriate level, not simply to deliver charge. The Court replaces that part of ST's proposed construction in order to more accurately describe the first gate drive circuit's purpose.

A Positive Supply Voltage

The Court adopts Motorola's construction and construes "a positive supply voltage" as "a voltage at an external source to the gate drive circuits that has a positive potential relative to a reference potential." Motorola's construction is consistent with the appropriate dictionary definition and is supported by the specification. Moreover, the Court finds that Motorola's construction more clearly defines the term's boundaries than ST's proposal.

Utilizes a First Charge Current

The Court adopts ST's proposal and construes the term "utilizes a first charge current" as "using a first current for charging the gate of a MOS power transistor." Motorola's construction differs only in that it requires a "charge pump."[11] As discussed *supra*, the Court declines to insert the term "charge pump" into this patent's construction.

A Second Gate Drive Circuit for Charge Pumping the Node

For reasons discussed regarding the term "a first gate drive circuit for charge pumping a node," the Court construes the term "a second gate drive circuit for charge pumping the node" as "a second circuit that drives a power transistor by raising the electrical potential in an additive, charge

[11]Motorola's proposed construction is: "applies current from a first charge pump to the gate of a MOS power transistor."

transfer process in the manner of a pump."

Utilizes a Second Charge Current

For reasons discussed regarding the term "utilizes a first charge current," the Court construes the term "utilizes a second charge current" as "using a second current for charging the gate of a MOS power transistor."

Enables the First and Second Gate Drive Circuits

The Court declines to construe the term "enables the first and second gate drive circuits" because the term is clear on its face.

Disables the First Gate Drive Circuit

The Court declines to construe the term "disables the first gate drive circuit" because the term is clear on its face.

Utilizing a First Charge Current

The Court declines to construe the term "utilizing a first charge current" because the term is clear on its face.

Utilizing a Second Charge Current

The Court declines to construe the term "utilizing a second charge current" because the term is clear on its face.

THE `563 DAVIES PATENT

The Davies patent discloses a semiconductor device configuration to achieve low source inductance. Inductance in a semiconductor device is undesirable because it limits the electrical current which can flow through the device at high frequencies. The Davies patent discloses structures common to all metal-oxide-semiconductor-field-effect-transistor ("MOSFET") devices:

source, drain, channel, and gate regions. According to the specification, it is desirable to connect the source region with the back side of the device (via the substrate) because: the source may be easily grounded to the heatsink; the heatsink will conduct heat away; and the configuration would eliminate the need for expensive and toxic beryllium oxide. However, connecting the source regions directly to the substrate can cause high source inductance, which is undesirable. Thus, the Davies innovation is to connect many source regions to a single "P+" region that is in turn connected to the substrate. This configuration allows for the benefits of connecting the source regions to the substrate without high source inductance.

Epitaxial Layer

The parties agreed to "epitaxial layer's" construction at the *Markman* hearing. The Court accepts the parties' agreement and accordingly construes the term as "a crystalline structure."

First Regions of the First Conductivity Type Formed in the Epitaxial Layer Extending Down to the Substrate

The Court agrees with Motorola and finds that the term "first regions of the first conductivity type formed in the epitaxial layer extending down to the substrate" does not need construction. Although the term is perhaps not simple, the individual words in the term have agreed or common meanings that are not in need of further construction. For example, the meanings of "first conductivity type," "epitaxial layer," and "substrate" are not in dispute. Additionally, the parties do not argue that "first region" is unclear in any way. And finally, despite ST's proposed construction, the Court finds that "extending down to" does not require construction.

Furthermore, the Court rejects ST's proposed construction because it improperly attempts to resolve the factual question raised by "extends down to." ST's proposed construction declares

"the first region has a boundary that reaches the substrate, the boundary being defined where the first region's dopant concentration equals the constant dopant concentration in the epitaxial layer." The term "extending down to" is plainly understood by those reasonably skilled in the art without need of construction. Thus, in a two-step infringement analysis,[12] it will be for the jury to determine whether the "first regions. . . [extend] down to the substrate." By strictly defining the first region's boundary, ST's proposed construction would improperly limit the facts the jury could consider to determine whether the infringing devices first region "extends down to" the substrate. There is no indication that the patentee intended to so limit the term and it is thus improper at the claim construction stage to prospectively constrain the jury's role in determining infringement.

Wherein the Plurality of First Regions and the Plurality of Source Regions are Connected Through an Ohmic Conductive Means

The Court adopts ST's proposed construction of the term "wherein the plurality of first regions and the plurality of source regions are connected through an ohmic conductive means" and construes the term as "wherein the plurality of first regions and the plurality of source regions are connected through a structure that provides a low resistance connection." The phrase "wherein the plurality of first regions and the plurality of source regions are connected" is clear on its face without further construction. Moreover, the parties agree that "an ohmic conductive means" is a structure that provides a low resistance connection.[13] Furthermore, the Court rejects Motorola's proposed construction for interjecting the term "cell" which itself would require construction.

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[12] *Liquid Dynamics Corp. v. Vaughan Co., Inc.*, 355 F.3d 1361, 1367 (Fed. Cir. 2004) (holding that infringement is a two-step analysis where the court first interprets claims' scope and meaning and the factfinder then compares properly construed claims to the allegedly infringing device).

[13] Motorola's proposed construction is: "in a plurality of cells each cell has a structure that provides a low resistance connection between the first region and the source region."

First Region of the First Conductivity Type Formed in the Epitaxial Layer, Extending from the Top Surface Down to the Substrate

For reasons discussed regarding the term "first regions of the first conductivity type formed in the epitaxial layer extending down to the substrate," the Court finds that "first region of the first conductivity type formed in the epitaxial layer, extending from the top surface down to the substrate" is clear on its face and does not require further construction.

First

The term "first" requires the Court to consider its authority to correct claim terms. When the Davies patent issued, claim 4 read in relevant part,

> a source and a drain region of a second conductivity type formed in the epitaxial layer extending from the top surface down into a portion of the epitaxial layer, wherein the source and drain regions are shallower than the second region and the source and drain regions are separated by the gate region, and further wherein the source region is formed inside the second region and the first region is shorted to the source region, *and wherein the drain region is adjacent to the first region*.

`563 Patent, 4:30-39 (emphasis added). Motorola argues that the word "first" in the last clause of claim 4 (italicized above) should be changed to "second." Motorola is not truly requesting a construction to clarify the meaning of "first" because the word "first" is clear on its face. Rather, Motorola argues that "first" is a typographical error that the Court should correct with the word "second." Although ST implicitly concedes that "first" is an error, ST argues that the error is beyond the Court's authority to correct.

A certificate of correction issued by the United States Patent and Trademark Office ("USPTO") perhaps supports Motorola's position. On July 29, 2003 Motorola obtained a certificate of correction declaring "Column 4, Line 23, replace 'first' with – second–." However, the certificate

of correction is itself flawed in that column 4, line 23 of the Davies patent does not contain the word "first." Motorola argues that the certificate of correction also contains a typographical error and should read "Claim 4, Line 23, replace 'first' with – second–." Thus construed, the certificate of correction addresses the relevant final clause of claim 4, and supports the conclusion that "first" should be replaced with "second."

The Court first considers whether the certificate of correction issued timely enough to be considered in this lawsuit. *Southwest Software, Inc. v. Harlequin Inc.* mandates that a " certificate of correction is only effective for causes of action arising after it was issued." 226 F.3d 1280, 1294 (Fed. Cir. 2000). In *Southwest Software*, Southwest sued Harlequin for infringement on January 20, 1995. *Id*. at 1287. Subsequently, in August of 1996, Harlequin noted that a necessary appendix was missing from one of the patents-in-suit and filed for summary judgment. *Id*. Thereafter, Southwest requested a certificate of correction from the PTO to add the certificate of correction, and the PTO issued said certificate on April 1, 1997. *Id*. at 1287, 1293-94. On appeal, the Federal Circuit considered whether the certificate of correction was to be considered for a cause of action that arose before its issuance. *Id*. at 1293-94. The Federal Circuit examined 35 U.S.C. § 254, which declares in relevant part "every such patent [patents having a certificate of correction], together with such certificate, shall have the same effect and operation of law on the trial of actions *for causes thereafter arising* as if the same had been originally issued in such corrected form." *Id*. at 1295 (emphasis added by prior court). The Court then found that under the statutory language,

> [F]or causes of action arising after the PTO issues a certificate of correction, the certificate of correction is to be treated as part of the original patent – i.e., as if the certificate had been issued along with the original patent. By necessary implication, for causes of action arising before its issuance, the certificate of correction is not effective."

Id.

Under *Southwest Software*, the relevant inquiry for considering a certificate is the date the cause of action arose. Although *Southwest Software* factually involved a certificate of correction issued after suit was filed, for several reasons, the Federal Circuit's holding turns on when the cause of action arose rather than when suit was filed. First, the language of 35 U.S.C. § 254 refers to the date a cause of action "arose," not the date a party filed suit. Second, the Federal Circuit never indicated an intention to limit its holding to the case's specific facts, but rather continually referred to the date the cause of action arose. *See e.g.*, *Southwest Software, Inc.*, 226 F.3d at 1295 ("for causes of action arising after the PTO issues a certificate of correction. . ."). And third, because patents and certificates of correction are meant to put the public on notice of what activities would infringe, it would be illogical to enforce certificates of correction against activity that occurred before the certificate issued. As the Federal Circuit declared in *Southwest Software*

> Until the PTO issues a certificate of correction pursuant to 35 U.S.C. § 254 adding the corresponding structure, such a claim would appear invalid to the public, and reasonable competitors would be justified in conducting their affairs accordingly. In such a case, where the claim is invalid on its face without the certificate of correction, it strikes us as an illogical result to allow the patent holder, once the certificate of correction has issued to sue an alleged infringer for activities that occurred before the issuance of the certificate of correction.

Id. at 1295-96.

Under the facts currently before the Court, the Court finds that the cause of action arose before the certificate issued. In the present case, ST filed suit on July 18, 2003, the USPTO issued the certificate of correction on July 29, 2003, and Motorola asserted the Davies patent in a counterclaim on September 11, 2003. Although it is possible that Motorola's cause of action for infringement of the Davies patent arose in the one and a half months between the certificate's issuance and the relevant counterclaim, the Court makes a factual determination that the cause of action did not. First, the certificate of correction appears to have been obtained solely for this

litigation because it was issued 11 years after the Davies patent was issued and sought only after ST had originally filed suit against Motorola. Such delay suggests that after ST filed suit: Motorola investigated ST products, then discovered potential infringement, then discovered the patent's error, and then requested a certificate of correction. Second, considering the complexity of the technology at issue, the Court finds it highly unlikely that in the one and a half months between the certificate's issuance: the accused infringer (ST) began infringing, Motorola discovered the infringement, and Motorola subsequently had time to draft and assert a counterclaim for infringement. Third, the parties have presented no evidence that Motorola's cause of action arose before the certificate of correction issued. On the evidence currently available, the Court makes a factual finding that Motorola's cause of action arose before the certificate of correction issued.[14] Accordingly, under *Southwest Software*, the Court gives no effect to the certificate of correction in this lawsuit. *Id*. at 1294.

Because the Court gives no effect to the certificate of correction, the Court's authority to correct the patent is unquestionably governed by *Novo Indus., L.P. v. Micro Molds Corp.*, 350 F.3d 1348, 1354 (Fed. Cir. 2003). The issue before the *Novo Industries* court was "whether a district court can act to correct an error in a patent by interpretation of the patent where no certificate of correction has been issued." *Id*. The Federal Circuit held "that the district court can correct only *Essex*[15]-type errors. A district court can correct a patent only if (1) the correction is not subject to reasonable debate based on consideration of the claim language and the specification and (2) the

[14]The Court recognizes that it may not have all relevant facts and is willing to revisit this factual finding if the parties have evidence establishing that Motorola's cause of action for infringement arose after the certificate of correction issued.

[15]*I.T.S. Rubber Co. v. Essex Rubber Co.*, 272 U.S. 429 (1926).

prosecution history does not suggest a different interpretation of the claims." *Id*. at 1357. Accordingly, the Court analyzes Motorola's request to correct the patent's error under the two-part *Novo Industries* test with *Essex* lending guidance for the test's application.

Both *Novo Industries* and *Essex* indicate that a proposed correction is subject to reasonable debate if more than one term can correct the problem. In *Novo Industries*, disputed claim 13[16] read in relevant part "(g) *stop means formed on a rotatable with said support finger* and extending outwardly therefrom into engaging relation with one of two spaced apart stop members formed on said frame." *Id*. at 1352 (emphasis added by prior court). The parties disputed the meaning of "a rotatable with" and the patentee argued that it could be corrected by either deleting "a rotatable with" or deleting "with said." *Id*. The district court rejected the proposed constructions and construed the term as "the mechanism for stopping the rotation of the drive gear is a part which is formed on *and* is rotatable with (rotates in unison with) the support finger." *Id*. at 1353 (emphasis added by prior court). Thus, the facts before the court were that the claim had a typographical error on its face and more than one correction, consistent with the intrinsic evidence[17], would cure that facial error. *Id*. at 1357. The Federal Circuit held that the correction was subject to reasonable debate, and thus the district court was without power to correct the term, because more than one correction would fix the error. *Id*. Even though all of the corrections were consistent with the specification, no one correction was clear enough "to overcome the ambiguity of the claim." *Id*.

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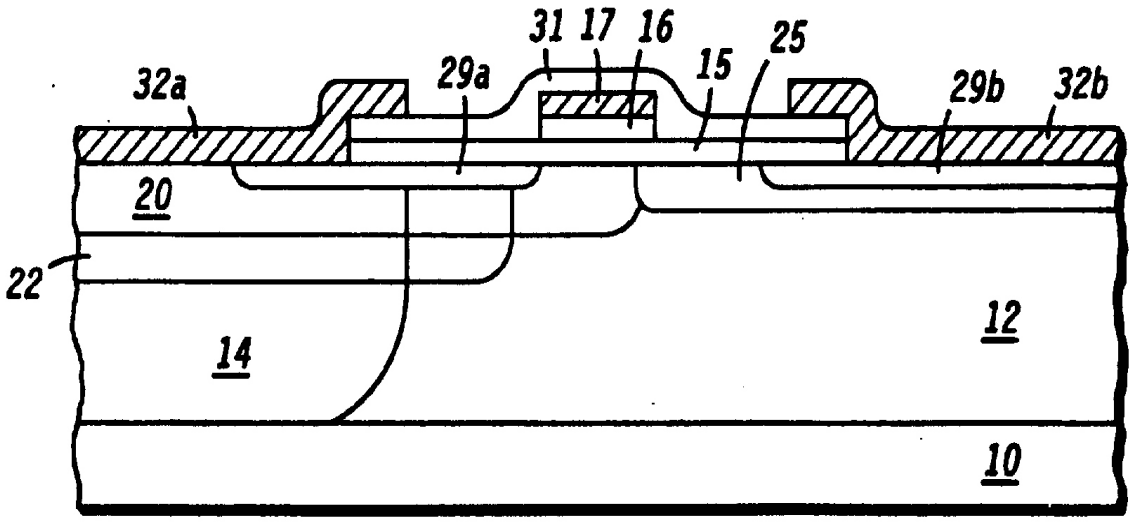
[16]Note that even though the claim cited here as "claim 13" is sometimes numbered 19 in the *Novo Industries* opinion, the *Novo Industries* opinion later makes clear that claim 19 became claim 13 in the issued patent. *Novo Industries, L.P.*, 350 F.3d at 1352 ("The examiner allowed claim 19, which became claim 13 of the issued patent.").

[17]A proposed correction that is inconsistent with the specification would amount to no correction at all, and would be contrary to *Essex*. *See Essex Rubber Co.*, 272 U.S. at 442 (holding it appropriate to correct the patent consistently with the specification).

Novo Industries and *Essex* indicate that the "no reasonable debate" standard is difficult to overcome. The Court finds it significant that the Federal Circuit did not parse hairs over which proposed correction best matched the specification. Instead, that court simply declared that even though the proposed corrections did not contradict the specification none resolved the ambiguity. *Id*. Moreover, the *Essex* facts support the conclusion that "no reasonable debate" is a difficult standard to meet. In *Essex*, although the term "rear upper edge" appeared in several claims, one claim omitted the word "rear." *Essex Rubber Co.*, 272 U.S. at 435, 441. The Court allowed addition of "rear" because: in prosecution, the patent applicant did not call attention to the omission and did not differentiate the claim with the omitted term to avoid reference to a prior art patent; the applicant did not object to the examiner's statement that the claim which omitted "rear" from "rear upper edge" in fact "specified a plane tangent to 'the rear upper edge;'" and the opposing party in the motion to dismiss proceedings recognized that the clause with the omitted word read the same as the other claims and did not change its position until after an appellate court called attention to the omission of "rear."[18] *Id*. at 441-42. Therefore, where more than one proposed correction is consistent with the specification, a correction is "not subject to reasonable debate" only where the specification makes one correction clearly correct. District courts should not adopt one correction over another simply because one more closely matches the specification.

[18]The Court recognizes that the relevant *Essex* facts listed in this sentence are perhaps more relevant to the second prong of *Novo Industries* concerning prosecution history. However, in many respects the two prongs of *Novo Industries* analytically overlap and the Court includes the relevant *Essex* facts to illustrate the difficulty in reaching the "no reasonable debate" bar.

In the instant case, the Court finds that there is more than one possible correction for the error found in claim 4 of the Davies patent and that Motorola's proposed correction is not clear enough to present "no reasonable debate." The illustration of the preferred embodiment from the Davies patent illustrates the two possible corrections.



As noted *supra*, the claim language in need of correction declares "wherein the drain region is adjacent to the first region." In the preferred embodiment as illustrated here: regions 25 and 29b constitute the "drain region"[19]; region 14 constitutes the "first region"[20]; region 20 constitutes the "second" or "channel" region[21]; and regions 15, 16, and 17 constitute the "gate region."[22] As both parties agree, claim 4 is facially incorrect because the drain region (25 and 29b) is not adjacent to

[19] '563 Patent, 3:15-17.

[20] '563 Patent, 2:5-14, 3:7, 3:42-44.

[21] '563 Patent, 2:30-35, 3:7, 3:23.

[22] '563 Patent, 2:14-22, 3:26-30.

the first region (14). Motorola asks the Court to rewrite "wherein the drain region is adjacent to the first region" as "wherein the drain region is adjacent to the second region" because drain region (25 and 29b) are adjacent to second region (20). Although Motorola is correct that the drain region is adjacent to the second region, the Court could also rewrite "wherein the drain region is adjacent to the first region" as "wherein the drain region is adjacent to the gate region" consistently with the specification because drain region (25 and 29b) is adjacent to gate region (15, 16, and 17). Moreover, replacing "first" with "gate" would not be facially inconsistent with claim 4 because claim 4 makes reference to the gate region. `563 Patent, 4:34-36 ("the source and the drain regions are separated by the gate region"). Importantly, Motorola has not presented any evidence which indicates that the patent requires "first" to be replaced with "second" beyond any reasonable debate. This is not like *Essex* where the circumstances unambiguously indicated one possible correction. The Court may not debate whether "second" is a more appropriate correction than "gate," because both are at least "reasonable."[23] As such, Motorola fails to meet the first prong of the *Novo Industries* test and the Court may not correct the patent's error.[24]

THE `654 TOBIN PATENT

The Tobin patent discloses a process that removes surface impurities from silicon wafers to be used in semiconductor devices. The Tobin patent's process involves heating the silicon wafer in

[23]The Court notes that support for replacing "first" with "gate" is weak at best. However, the argument that "first" may be replaced with "gate" is at least "reasonable."

[24]Additionally, even though the Court need not address the second prong of *Novo Industries*, the Court notes that under the submitted briefing, the court must find that the prosecution history does not preclude modifying the term "first." The only prosecution history presented to the Court is the certificate of correction issued after the cause of action arose. The certificate of correction constitutes no prosecution history because, as discussed *supra*, the Court may not consider that certificate in this action. *Southwest Software, Inc. v. Harlequin Inc.*, 226 F.3d 1280, 1294 (Fed. Cir. 2000). Thus, the Court presumes that there is no relevant prosecution history that would "suggest a different interpretation of the claims."

a "reducing ambient," such as hydrogen gas. As the wafer is heated, oxygen diffuses out of the silicon wafer into the ambient, and, in the preferred embodiment, hydrogen from the reducing ambient diffuses into the silicon wafer. As a result, the surface layer of the silicon wafer contains relatively little oxygen. The process then continues by lowering the temperature. This in turn causes oxygen in the silicon wafer's lower layers to precipitate into "gettering sites." These "gettering sites" are desirable in the lower layers of the silicon wafer.

Reducing Ambient

The Court adopts Motorola's proposed construction and construes the term "reducing ambient" as "a gaseous atmosphere that adds an electron to an element or compound." The parties agree that a "reducing ambient" is a gaseous atmosphere that "adds" or "donates" electrons. The only discrepancy between the parties' constructions is ST's assertion that in a "reducing ambient," the "principal reactant gas" must be a "chemical" and that the electrons must be donated in a "chemical reaction." The Court finds that specification and claims do not so limit the definition of "reducing ambient." *See Sunrace Roots Enter. Co., LTD v. SRAM Corp.*, 336 F.3d 1298, 1303-1304 (Fed. Cir. 2003). In the Tobin Patent, a "reducing ambient," as Motorola proposes, is simply a gaseous atmosphere that adds electrons to some element or compound. Whether, in a particular circumstance, a chemical reaction is or is not the means by which those electrons are added is a question of infringement properly for a jury to decide. *See Liquid Dynamics Corp. v. Vaughan Co., Inc.*, 355 F.3d 1361, 1367 (Fed. Cir. 2004) (holding that infringement is a two-step analysis where the court first interprets claims' scope and meaning and the factfinder then compares properly construed claims to the allegedly infringing device).

THE `798 QUAN PATENT

The Quan patent discloses methods for applying protective coverings to semiconductor devices. In the past, one common method for applying protective coverings to semiconductor devices was to directly dispense a liquid encapsulating material onto the device that would then harden into a protective covering. This so-called "glob top" method created a convex covering difficult for machines to handle and/or label. Another common method for applying a protective covering, the injection molding method, involved placing a formed mold over the semiconductor device and then injecting liquid encapsulating material into the mold. The injection molding process solved the convex covering problem associated with glob-top covering, but was also less efficient. Additionally, both methods were inefficient in that they involved encapsulating one semiconductor device at a time. To solve these problems, the Quan patent discloses methods whereby many semiconductor devices are encapsulated at the same time and then severed into individual, encapsulated devices. Additionally, the Quan patent discloses methods of encapsulating semiconductor devices to create a uniform surface.

Package

The Court construes the term "package" as "at least one electronic component or die covered by encapsulating material." Although the parties generally agree on the Court's proposed construction, the Court rejects both parties' proposed constructions because they include unwarranted limitations. First, ST's proposed construction[25] requires "external terminals to provide access to the components found inside." Although the Court would imagine that such terminals would exist on any such semiconductor device, the Court finds no language in the claims that

[25]ST's proposed construction is: "a protective container or housing for an electronic component or die, with external terminals to provide access to the components inside."

requires such terminals and finds no clear disavowal of claim scope in the specification. Moreover, Motorola's proposed construction[26] improperly incorporates the requirement of an "interconnect substrate" into the claims. Although the term "interconnect substrate" is mentioned in the description of one preferred embodiment, the specification does not exhibit a clear disavowal of claim scope or definition of the term such that the term "interconnect substrate" should be read into the claim. `798 Patent, 1:48-50.

Substrate

The Court adopts ST's proposed construction of the term "substrate" and construes the term as "a mechanical support for an electronic component, which can have a variety of forms, including a stamped leadframe, a ceramic substrate, a printed circuit board, and other known configurations."

Encapsulating

The Court finds that the term "encapsulating" is not in need of interpretation.

Top Surface Planarity Deviation

The Court adopts ST's proposed construction and construes the term "top surface planarity deviation" as "the difference between the average height of the entire top surface and the point most removed from the average." ST's proposed definition finds support from the McGraw-Hill Dictionary of Scientific and Technical Terms, which defines "deviation" as "the difference between any given number in a set and the mean average of those numbers." Additionally, the Court rejects Motorola's proposed construction, "statistical deviation of the average height of the top surface" because the term "statistical deviation" would itself require construction for the jury.

[26]Motorola's proposed construction is: "an interconnect substrate holding at least one electronic component covered by encapsulating material."

Overmolding

The Court adopts ST's proposed construction of the term "overmolding" and construes the term as "forming encapsulating material in a cavity of a defined shape over one or more components on only one side of a substrate." ST's proposed construction finds support from a relevant scientific dictionary and does not import unwarranted limitations into the claim term. Moreover, Motorola's proposed construction[27] is based on extrinsic expert testimony and imports the extraneous limitation of injecting material "under pressure" into the claim term.

THE `814 VAGLICA PATENT

The Vaglica patent discloses a system for debugging a data processor. Under the prior art, designers would often fix, or "debug," data processors by accessing the system's internal workings via normal system resources (e.g. a communication port). Under the Vaglica patent, the data processor has a normal mode of operation and a debugging mode of operation. In the normal mode of operation, the processor connects to system resources and operates much as any other data processor. However, in the debugging mode of operation, the data processor utilizes a separate communications bus to connect to the debugging system. Thus, a designer debugging the processor can connect directly to the processor without having to work through other system resources.

First and Second Modes of Operation

The Court finds that the term "first and second modes of operation" does not require construction.

Means for Operating a Serial Communication Bus

[27]Motorola's proposed construction is: "Molding by transferring or injecting an encapsulating material under pressure into a mold cavity covering one side of a substrate."

The Court adopts Motorola's proposed construction and construes the term "means for operating a serial communication bus" as "Background Mode Serial Logic (45) or Serial Interface (55)." In full, the disputed claim language reads:

> means for operating a serial communication bus, said serial communication bus is coupled to said data processor by means of a plurality of pins, each of said plurality of pins is either not used or is used only for development support functions while said data processor is in said first mode

`814 Patent, 13: 21-25. The parties agree that the term "means for operating a serial communication bus" is a means-plus-function limitation.[28] The Court agrees with Motorola that the function of the means-plus-limitation term is "operating a serial communication bus." Additionally, as the parties have agreed, the corresponding structure includes Background Mode Serial Logic (45) and Serial Interface (55) from the Vaglica patent's Figures 3 and 4. However, the Court rejects ST's proposed construction because ST has not established that the specification also "clearly links"[29] the bidirectional pin IFETCH/DSI, and pins IPIPE/DSO and BKPT/DSCLK with the "means for operating a serial communication bus."

Pins

The Court construes the term "pins" as "external connection points of a device." The Court finds that this construction comports with the relevant dictionary definitions submitted by the parties

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[28]The language cited from claim one in the previous sentence also contains the disputed terms "pins" and "development support functions." Although the initial term "means for operating a serial communication bus" is a means-plus-function limitation, the remainder of this cited language, including "pins" and "development support functions" is not a means-plus-function limitation. The word "means" in the remainder of the relevant claim language ("by means of a plurality of pins . . .") does not invoke 35 U.S.C. § 112 ¶ 6 because the remainder of the claim language recites structure rather than function. *York Prods., Inc. v. Central Tractor Farm & Family Center*, 99 F.3d 1568, 1574 (Fed. Cir. 1996). Therefore, the remainder of the claim language ("by means of a plurality of pins . . .") is an additional limitation on the means-plus-function limitation ("means for operating a serial communication bus") rather than another means-plus-function limitation itself.

[29]*Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001) (A "structure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim.").

and most accurately reflects the meaning as understood by one of ordinary skill in the art.

Development Support Functions

The Court adopts Motorola's proposed construction of the term "development support functions" and construes the term as "functions in support of a development system to debug hardware and/or software of the data processor." The Court finds that Motorola's proposed construction more accurately reflects a person of ordinary skill in the art's understanding. Additionally, the Court rejects ST's proposed construction because the Court does not find that the prosecution history warrants the additional limitations ST proposes.

Means for Sequentially Executing, While in Said First Mode, a First Plurality of Instructions Fetched From a Memory by Means of Said Parallel Communication Bus While in Said First Mode

The Court construes the means-plus-function term "means for sequentially executing while in said first mode, a first plurality of instructions fetched from a memory by means of said parallel communication bus while in said first mode" as "CPU (11) including IR PIPE 51, execution unit 52, sequencer 53, and microcode 54." Despite their briefing, the parties generally agree that the corresponding structure is CPU(11). The dispute between the parties is whether the proper construction is simply CPU (11) or also includes the constituent parts of CPU (11). Although the Court agrees that the corresponding structure is CPU (11), the Court finds that the patent also "clearly links or associates" other structures with CPU (11) that should be included in this term's construction. *See Medtronic, Inc. v. Advanced Cardiovascular Systems, Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001). Specifically, the specification declares that "FIG. 4 illustrates in greater detail the logical relationships between the major components of CPU 11 as they relate to the subject matter of the present invention." `814 Patent, 8:53-55. Accordingly, pursuant to Figure 4 and the relevant

specification language, the proper construction should include: IR PIPE 51, execution unit 52, sequencer 53, and microcode 54. Moreover, the Court rejects ST's request to include the limitation "this structure must execute only debug instructions in the debug mode, as indicated by the FREEZE signal" because ST has not established that the specification clearly links that limitation with the corresponding structure (CPU (11)). The Court also finds that the specification does not require ST's proposed limitation "and undisclosed additional decode circuitry."

Means for Sequentially Executing, While in Said Second Mode, a Second Plurality of Instructions Received by Means of Said Serial Communication Bus While in Said Second Mode

For the reasons stated in regards to the term "means for executing while in said first mode, a first plurality of instructions fetched from a memory by means of said parallel communication bus while in said first mode," the Court construes the means-plus-function term "means for sequentially executing" from the claim language "means for sequentially executing, while in said second mode, a second plurality of instructions received by means of said serial communication bus while in said second mode" as "CPU (11) including IR PIPE 51, execution unit 52, sequencer 53, and microcode 54."

Means for Accessing Said Memory by Means of Said Parallel Communication Bus While in Said Second Mode

The Court construes the means-plus-function limitation "means for accessing said memory by means of said parallel communication bus while in said second mode" as "IMB (12) and Bus Controller (40/50)."

Mode Switch Means for Switching Between Said First and Second Modes and for Disabling Said Means for Operating a Serial Communication Bus While Said Data Processor is in Said First Mode

The Court adopts Motorola's proposed construction of the means-plus-function term "mode switch means for switching between said first and second modes and for disabling said means for operating a serial communication bus while said data processor is in said first mode" and finds that the corresponding structure is "structure responsive to BKPT (in bus controller 50), to background instruction, or to double bus faults; logic that asserts FREEZE signal; instruction to resume normal mode; logic for latching the state of the BKPT signal."

Said Mode Switch Means is Responsive to an Externally Provided Signal to Switch From Said First Mode of Operation to Said Second Mode of Operation

The Court finds that this term from Claim 3 of the Vaglica patent is not a means-plus-function limitation as ST argues, but rather is an additional limitation on a previously defined means-plus-function limitation. Consequently, as the parties have agreed, this term is not in need of construction.

Control Means for Disabling Said Mode Switch Means From Switching to Said Second Mode of Operation

The Court agrees with Motorola that this term's construction is governed by the construction of "mode switch means for switching between said first and second modes and for disabling said means for operating a serial communication bus while said data processor is in said first mode" and accordingly finds that the corresponding structure of this means-plus-function limitation is "logic for latching the state of the BKPT signal."

First Means for Executing Said Instructions

Because the parties agree that the construction of "first means for executing said instructions" mirrors the construction of the term "means for executing while in said first mode, a first plurality

of instructions fetched from a memory by means of said parallel communication bus while in said first mode," the Court adopts the same reasoning and construction for the means-plus-function term "first means for executing said instructions" and finds that the corresponding structure is "CPU (11) including IR PIPE 51, execution unit 52, sequencer 53, and microcode 54."

Third Means for Providing Access to at Least One of the System Resources in Accordance With the Execution by Said First Means of a Second Subset of Said Instructions

The Court adopts Motorola's proposed construction and finds that the corresponding structure of this means-plus-function term is "IMB (12), Bus Controller (40/50), Background Mode Serial Logic (45) or Serial Interface (55)."

First Communication Means for Providing Instruction of Said First Subset to Said First Means, Said First Communication Means is Operative for Communication in Response to Instructions of Both Said First and Second Subsets of Instructions

The Court adopts Motorola's proposed construction of this means-plus-function term and finds that the corresponding structure is "IMB (12); Bus Controller (40/50)."

Second Communication Means Distinct From Said First Communication Means for Providing Instructions of Said Second Subset to Said First Means, Said Second Communication Means is not Operative for Communication of Instructions of Said Second Subset in Response to Any Instructins of Said First Subset of Instructions

The Court adopts Motorola's proposed construction of this means-plus-function limitation and finds that the corresponding structure is "Background Mode Serial Logic (45); Serial Interface (55); IPIPE/DSO, IFETCH/DSI, BKPT/DSCLK."

Mode Switch Means for Switching Between Said First and Second Subsets of Said Instructions, Said

Mode Switch Means Being Responsive to an Externally-Provided Signal to Switch From Said First Subset to Said Second Subset

The Court adopts Motorola's proposed construction of this means-plus-function limitation and finds that the corresponding structure is "structure responsive to BKPT (in bus controller 50), to background instruction, or to double bus faults; logic that asserts FREEZE signal; instruction to resume normal mode."

Control Means for Disabling Said Mode Switch Means From Switching to Said Second Subset of Said Instructions

The Court adopts Motorola's proposed construction of this means-plus-function limitation and finds that the corresponding structure is "logic for latching the state of the BKPT signal."

Execution Means for Sequentially Executing a Plurality of Instructions, Said Execution Means Having a First Mode in Which Instructions of a first subset are Executed and a Second Mode in Which Instructions of a Second Subset are Executed

The Court finds that "execution means for sequentially executing a plurality of instructions" is a means-plus-function limitation, and that the balance of this term is a further limitation on the means-plus-function limitation rather than a means-plus-function limitation itself. Additionally, the Court finds that "execution means for sequentially executing a plurality of instructions" should be construed consistently with "first means for executing said instructions" from Claim 8, and consequently that the corresponding structure is "CPU (11) including IR PIPE 51, execution unit 52, sequencer 53, and microcode 54."

Communication Means for Providing Said Plurality of Instructions to Said Execution Means, Said Communication Means Operating in a Master Mode While Providing Instructions of Said First

Subset and in a Slave Mode While Providing Instructions of Said Second Subset

As the parties have agreed, the Court finds that the term "communication means for providing said plurality of instructions to said execution means" is a means-plus-function limitation. The Court rejects ST's argument that the following language from claim 13 "said communication means uses the first plurality of pins while providing instructions of the first subset and uses the second plurality of pins while providing instructions of the second subset, each of the second plurality of pins is either not used or is used only for development support functions while the communication means is providing instructions of the first subset" is also a means-plus-function limitation. That language is merely a structural limitation on the prior means-plus-function limitation "communication means for providing said plurality of instructions to said execution means." *York Prods., Inc. v. Central Tractor Farm & Family Center*, 99 F.3d 1568, 1574 (Fed. Cir. 1996). Consequently, the Court adopts Motorola's proposed construction and finds that the corresponding structure is "IMB (12); Bus Controller (40/50); Background Mode Serial Logic (45); Serial Interface (55)."

Mode Switch Means for Switching Between Said First Mode and Said Second Mode and for Preventing Said Communication Means from Operating in Said Slave Mode While Said Execution Means is Executing Instructions of Said First Subset

Because the parties agree that this means-plus-function limitation should be construed consistently with the means-plus-function term "mode switch means for switching between said first and second modes and for disabling said means for operating a serial communication bus while said data processor is in said first mode" the Court finds that the corresponding structure is "structure responsive to BKPT (in bus controller 50), to background instruction, or to double bus faults; logic

that asserts FREEZE signal; instruction to resume normal mode; logic for latching the state of the BKPT signal."

Said Mode Switch Means is Responsive to an Externally Provided Signal to Switch From Said First Mode to Said Second Mode

The Court finds that this is not a means-plus-function limitation but is rather an additional limitation on a prior means-plus-function limitation. *Id.* Accordingly, no construction is necessary.

Control Means for Disabling Said Mode Switch Means From Switching to Said Second Mode of Operation

Because the parties agree that this term should be construed consistently with "control means for disabling said mode switch means from switching to said second subset of said instructions" from claim 3, the Court adopts Motorola's proposed construction of this means-plus-function limitation and finds that the corresponding structure is "logic for latching the state of the BKPT signal."

So **ORDERED** and **SIGNED** this 15 day of **July, 2004.**

LEONARD DAVIS
UNITED STATES DISTRICT JUDGE

APPENDIX A: CLAIM CONSTRUCTION CHART

ST INC's '789 Patent (Diaz et al.)	
Claim	**Court's Construction**
1. An electronic system coupled to a memory, comprising:	
a first device that requires access to the memory;	
a decoder that requires access to the memory sufficient to maintain **real time operation**; and	Processing fast enough to keep up with an input data stream.
a **memory interface** for coupling to the memory, and coupled to the first device and to the decoder,	[AGREED] A device or boundary that couples the memory with one or more other devices that require access to the boundary.
the memory interface having an **arbiter**	[AGREED] A device that used a priority scheme to determine which requesting device will gain access to the memory.
for **selectively providing access** for the first device and the decoder to the memory and	Determining which of a plurality of devices coupled to a bus is allowed access to the memory based on a priority scheme.
a **shared bus** coupled to the memory the first device, and the decoder,	[AGREED] A signal or set of signal lines to which a number of devices are coupled and over which information may be transferred between them.
the bus having a **sufficient bandwidth** to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.	Sufficient data transfer capability.

APPENDIX A: CLAIM CONSTRUCTION CHART

ST INC's '092 Patent (Edwards et al.)	
Claim	**Court's Construction**
23. A microcomputer comprising an on-chip processor and an on-chip **writable memory** on a single integrated circuit chip having	Memory that is capable of having data written to and read from.
a **substrate of semiconductor material of a first type**, wherein said on-chip writable memory comprises	The base layer of an integrated circuit doped to be either p-type or n-type.
a **high density memory array** having at least 1K bytes for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	A memory array having a large number of memory cells for a given area.
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	
(d) a plurality of on-chip transistors comprising **circuitry operable independently of the operation of said memory array**,	Circuitry whose operation is not contingent upon operation of the memory array.
(e) a first **isolation region in said substrate**, said first isolation region containing all of said memory cells of said high density memory array, and	Region in the substrate isolated from noise generated in another region.

APPENDIX A: CLAIM CONSTRUCTION CHART

ST INC's '092 Patent (Edwards et al.)	
Claim	**Court's Construction**
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array, said **first and second regions noise isolated from each other**,[30]	First and second regions, each region isolated from noise produced in the other region.
whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from **noise**	Unwanted electrical signals.
[noise] due to independent operation of said transistors.	Noise caused by operation of a plurality of on-chip transistors whose operation is not contingent upon operation of the memory array.

[30] The parties have agreed that **"noise isolated"** means "isolated from noise produced in another region."

APPENDIX A: CLAIM CONSTRUCTION CHART

ST INC's '244 Patent (Hopkins)	
Claim	**Court's Construction**
1. A circuit for driving a MOS power transistor, comprising: **a first gate drive circuit for charge pumping a node** connected to a gate of the MOS power transistor to a gate supervoltage higher than	A first circuit that drives a power transistor by raising the electrical potential in an additive, charge transfer process in the manner of a pump.
a positive supply voltage by at least an amount equal to	A voltage at an external source to the gate drive circuits that has a positive potential relative to a reference potential.
a **threshold voltage** of the MOS power transistor,	[AGREED] The minimum voltage applied to the gate of a transistor, with respect to the source, necessary for the onset of current flow between drain and source
wherein the first gate drive circuit **utilizes a first charge current** to charge the MOS power transistor gate to the gate supervoltage at a first rate;	Using a first current for charging the gate of a MOS power transistor.
a second gate drive circuit for charge pumping the node connected to the gate of the MOS power transistor to maintain the voltage on such node at the gate supervoltage,	A second gate drive circuit for charge pumping the node" as "a second circuit that drives a power transistor by raising the electrical potential in an additive, charge transfer process in the manner of a pump.
wherein the second gate drive circuit **utilizes a second charge current**, less than the first charge current, to charge the MOS power transistor gate to the gate supervoltage at a second rate which is slower than the first rate; and	Using a second current for charging the gate of a MOS power transistor.
a control circuit, wherein the control circuit **enables the first and second gate drive circuits** when the MOS power transistor is initially turned on, and thereafter	Enables the first and second gate drive circuits.
disables the first gate drive circuit after a selected period of time.	Disables the first gate drive circuit

APPENDIX A: CLAIM CONSTRUCTION CHART

ST INC's '244 Patent (Hopkins)	
Claim	**Court's Construction**
13. The circuit of claim 1, further comprising **means for connecting the gate of the MOS power transistor to ground**, wherein the MOS power transistor can be turned off when desired.	[AGREED] This claim element is in means-plus-function form under 35 U.S.C. § 112(6). The corresponding structure is CTRL signal on line 22 and the switch element represented by block 65 in Fig. 1 or CTRL signal on line 78 and the switch element represented by block 115 in Fig. 2.
14. A method for driving a MOS power transistor, comprising the steps of: when the MOS power transistor is turned on, charging a node connected to a gate thereof to a gate supervoltage higher than a positive supply voltage by at least an amount equal to a threshold voltage of the MOS power transistor, **utilizing a first charge current** to charge the node at a first rate; and	Utilizing a first charge current.
after a predetermined time period, maintaining the voltage on the node at the gate supervoltage **utilizing a second charge current**, less than the first charge current, to charge the MOS power transistor gate to the gate supervoltage at a at a second rate, wherein said second rate is slower than said first rate.	Utilizing a second charge current.
15. The method of claim 14, wherein said step of charging the node connected to the gate thereof at the first rate comprises charging the node using a first and a second gate drive circuit.	

APPENDIX A: CLAIM CONSTRUCTION CHART

Motorola's '563 Patent (Davies et al.)	
Claim	**Court's Construction**
1. A semiconductor device, comprising:	
a substrate of **a first conductivity type**;	Conductivity associated with conduction of charges in a semiconductor, either n-type or p-type.
an **epitaxial layer** of the first conductivity type	A crystalline structure.
formed on the substrate;	Created by introducing material on or in.
a **plurality** of channel regions of the first conductivity type	Two or more.
formed in the epitaxial layer;	Add dopant atoms in an area to create a region therein
a plurality of source and drain regions of a **second conductivity type** formed in the epitaxial layer, wherein the source regions are	The conductivity type opposite to that of the "first conductivity type," as defined above.
within the channel regions and the drain regions are	Inside the channel regions.
adjacent to the channel regions and spaced from the source regions; and	Abutting or next to.
a plurality of **first regions of the first conductivity type formed in the epitaxial layer extending down to the substrate**,	No construction necessary.
wherein the first regions are partially overlapping the source regions and the channel regions, and	
wherein the plurality of first regions and the plurality of source regions are connected through an ohmic conductive means.	Wherein the plurality of first regions and the plurality of source regions are connected through a structure that provides a low resistance connection.

APPENDIX A: CLAIM CONSTRUCTION CHART

Motorola's '563 Patent (Davies et al.)	
Claim	**Court's Construction**
2. The semiconductor device of claim 1 wherein a maximum of two sources regions each	
are **connected through**	Electrically connected via.
ohmic means with one first region.	A structure that provides a low resistance connection.
4. A semiconductor device, comprising:	
a substrate of a first conductivity type;	
an **epitaxial layer** of the first conductivity type	A crystalline structure.
disposed on the substrate, wherein the epitaxial layer has a top surface and a bottom surface;	Formed on; see the construction for "formed on" above.
a **first region of the first conductivity type formed in the epitaxial layer, extending from the top surface down to the substrate**,	No construction necessary.
wherein the first region is more heavily doped than the epitaxial layer;	
a second region of the first conductivity type formed in the epitaxial layer, extending from the top surface down into a portion of the epitaxial layer;	
a gate region disposed on the epitaxial layer; and	

APPENDIX A: CLAIM CONSTRUCTION CHART

Motorola's '563 Patent (Davies et al.)	
Claim	**Court's Construction**
a source and a drain region of a second conductivity type formed in the epitaxial layer extending from the top surface down into a portion of the epitaxial layer, wherein the source and drain regions are shallower than the second region and the source and the drain regions are separated by the gate region, and further wherein the source region is formed inside the second region and the first region is **shorted to** the source region, and	Electrically connected by a low resistance pathway.
wherein the drain region is **adjacent**	Abutting or next to.
the **first** region.	First
6. The semiconductor device of claim 4 wherein the drain region is comprised of a lightly doped region and a more heavily doped region.	

Motorola's '654 Patent (Tobin)	
Claim	**Court's Construction**
1. A process for preparing a **silicon substrate** for the fabrication of a device which comprises the steps of:	Silicon material on or in which semiconductor device elements are fabricated.
providing a silicon substrate having a concentration of oxygen incorporated therein;	
heating said substrate to a first elevated temperature in a **reducing ambient**;	A gaseous atmosphere that adds an electron to an element or compound.

APPENDIX A: CLAIM CONSTRUCTION CHART

Motorola's '654 Patent (Tobin)	
Claim	**Court's Construction**
lowering the temperature of said substrate to a second elevated temperature lower than said first elevated temperature; and	
maintaining said substrate at said second elevated temperature for a time to allow **nucleation** of	The creation of clusters.
oxygen precipitates in the bulk of said substrate.	Small clusters of oxygen-containing substances.
2. The process of claim 1 wherein said **reducing ambient** comprises hydrogen.	A gaseous atmosphere that adds an electron to an element or compound.
3. The process of claim 2 wherein said **reducing ambient** comprises hydrogen	A gaseous atmosphere that adds an electron to an element or compound.
diluted with argon or helium.	Made less concentrated.
4. The process of claim 1 wherein said concentration of oxygen exceed 1.3 X 10^{18} cm^{-3}.	
5. The process of claim 1 wherein said first temperature comprises a temperature between about 1000° C. and about 1200° C.	
6. The process of claim 1 wherein said second elevated temperature is about 600°–800° C.	
7. The process of claim 5 wherein said first temperature is about 1100°–1150° C.	

APPENDIX A: CLAIM CONSTRUCTION CHART

Motorola's '654 Patent (Tobin)	
Claim	**Court's Construction**
9. A process for fabricating a semiconductor device which comprises the steps of:	
providing a **silicon wafer** of	See the construction for "silicon substrate" as used in claim 1. The terms "silicon substrate" and "silicon wafer" are used interchangeably in the Tobin patent specification.
first conductivity type having a concentration of oxygen incorporated therein;	Conductivity associated with conduction of charges in a semiconductor, either n-type or p-type.
heating said wafer to a temperature between about 1000° and 1200° C. in a **reducing ambient** for a sufficient time to form a denuded surface layer on said wafer;	A gaseous atmosphere that adds an electron to an element or compound.
heating said wafer in an **oxidizing ambient** to form a protective oxide on the surface thereof;	A gaseous atmosphere in which the principal reactant gas is a chemical that accepts electrons in a chemical reaction.
reducing the temperature of said wafer to a second temperature between about 600° and 800° C. to nucleate the precipitation of oxygen in the bulk of said wafer; and	
forming regions of **second conductivity type** in said denuded surface layer, said regions having a depth into said wafer less than the thickness of said surface layer.	The conductivity type opposite to that of the "first conductivity type," as defined above.

APPENDIX A: CLAIM CONSTRUCTION CHART

Motorola's '798 Patent (Quan et al.)	
Claim	**Court's Construction**
1. A method of forming a semiconductor **package** comprising:	At least one electronic component or die covered by encapsulating material.
forming a **substrate** having a	A mechanical support for an electronic component, which can have a variety of forms, including a stamped leadframe, a ceramic substrate, a printed circuit board, and other known configurations.
plurality of package sites and	Two or more.
an **electronic component** attached to the plurality of package sites;	An electrical device or element, such as a semiconductor device, resistor or capacitor.
encapsulating the plurality of package sites wherein the encapsulating forms a continuous encapsulating material covering the plurality of package sites; and	Encapsulating.
singulating through the encapsulating material to	Separating.
singulate each package site into an individual package.	Separate.
2. A method of forming a semiconductor **package** comprising:	At least one electronic component or die covered by encapsulating material
encapsulating a plurality of package sites that are on a	Encapsulating.
substrate wherein	A mechanical support for an electronic component, which can have a variety of forms, including a stamped leadframe, a ceramic substrate, a printed circuit board, and other known configurations.

APPENDIX A: CLAIM CONSTRUCTION CHART

Motorola's '798 Patent (Quan et al.)	
Claim	**Court's Construction**
the encapsulating forms a continuous encapsulating material covering the plurality of package sites and wherein encapsulating the plurality of package sites includes forming the encapsulating material to have	
a **top surface planarity deviation** of less than 0.13 millimeters; and	The difference between the average height of the entire top surface and the point most removed from the average
singulating through the encapsulating material to	Separating.
singulate each package site.	Separate.
12. The method of claim 1 wherein **encapsulating** the plurality of package sites includes encapsulating by	Encapsulating.
overmolding.	Forming encapsulating material in a cavity of a defined shape over one or more components on only one side of a substrate

APPENDIX A: CLAIM CONSTRUCTION CHART

Motorola's '814 Patent (Vaglica)		
Claim	**Claim No.**	**Court's Construction**
1. A data processor having **first and second modes of operation** for use in a data processing system comprising:	1[A]	No construction necessary.
means for operating a parallel communication bus	1[B]	35 U.S.C. 112(6) Corresponding structure: Bus Controller (40/50)
means for operating a serial communication bus, said serial communication bus is coupled to said data processor by means of a plurality of pins, **each of said plurality of pins is either not used or is used only for development support functions while said data processor is in said first mode;**	1[C](i)	Corresponding Structure: Background Mode Serial Logic (45) or Serial Interface (55).
pins development support functions	1[C][ii]	external connection points of a device
the data processor comprising:	1[D]	Term not identified as needing construction.
means for sequentially executing, while in said first mode, a first plurality of instructions fetched from a memory by means of said parallel communication bus while in said first mode;	1[E]	Corresponding Structure: IMB (12) and Bus Controller (40/50)
means for sequentially executing, while in said second mode, a second plurality of instructions received by means of said serial communication bus while in said second mode, said means for executing a second plurality of instructions further comprising	1[F](i)	Corresponding Structure: IMB (12) and Bus Controller (40/50).

APPENDIX A: CLAIM CONSTRUCTION CHART

Motorola's '814 Patent (Vaglica)		
Claim	**Claim No.**	**Court's Construction**
means for accessing said memory by means of said parallel communication bus while in said second mode; and	1[F](ii)	Corresponding Structure: IMB (12) and Bus Controller (40/50).
mode switch means for switching between said first and second modes and for disabling said means for operating a serial communication bus while said data processor is in said first mode.	1[G]	Corresponding Structure: structure responsive to BKPT (in bus controller 50), to background instruction, or to double bus faults; logic that asserts FREEZE signal; instruction to resume normal mode; logic for latching the state of the BKPT signal.
3. A data processor according to claim 1 further comprising:	3[A]	Term not identified as needing construction.
said mode switch means is responsive to an externally-provided signal to switch from said first mode of operation to said second mode of operation;	3[B]	35 U.S.C. § 112 ¶ 6 does not apply. Therefore, term does not require construction.
control means for disabling said mode switch means from switching to said second mode of operation.	3[C]	Corresponding Structure: logic for latching the state of the BKPT signal.
8. A data processor for executing each of a plurality of instructions, the data processor having a plurality of system resources and comprising	8[A]	Term not identified as needing construction.
first means for executing said instructions;	8[B]	Corresponding Structure: CPU (11) including IR PIPE 51, execution unit 52, sequencer 53, and microcode 54
second means for utilizing the system resources in accordance with the execution by said first means of a first subset of said instructions	8[C]	35 U.S.C .§ 112(6) governs: The corresponding structure is same as for "means for operating a parallel communication bus" in 1[B] (i.e., bus controller 40 in Fig. 3 and 50 in Fig. 4).
third means for providing access to at least one of the system resources in	8[D]	Corresponding Structure: IMB (12), Bus Controller (40/50), Background Mode Serial

APPENDIX A: CLAIM CONSTRUCTION CHART

Motorola's '814 Patent (Vaglica)		
Claim	**Claim No.**	**Court's Construction**
accordance with the execution by said first means of a second subset of said instructions;		Logic (45) or Serial Interface (55).
first communication means for providing instructions of said first subset to said first means, said first communication means is operative for communication in response to instructions of both said first and second subsets of instructions;	8[E]	Corresponding Structure: IMB (12); Bus Controller (40/50).
second communication means distinct from said first communication means for providing instructions of said second subset to said first means, said second communication means is not operative for communication of instructions of said second subset in response to any instructions of said first subset of instructions; and	8[F]	Corresponding Structure: Background Mode Serial Logic (45); Serial Interface (55); IPIPE/DSO, IFETCH/DSI, BKPT/DSCLK.
fourth means coupled to said first means and to said second communication means **for using said second communication means to indicate a status of said first means while said first means is executing instructions of said first subset**.	8[G]	[AGREED] Corresponding structure: IPIPE and IFETCH.
10. A data processing system according to claim 8 further comprising:	10[A]	Term not identified as needing construction.
mode switch means for switching between said first and second subsets of said instructions, said mode switch means being responsive to an externally-provided signal to switch	10[B]	Corresponding structure: structure responsive to BKPT (in bus controller 50), to background instruction, or to double bus faults; logic that asserts FREEZE signal; instruction to resume normal mode.

APPENDIX A: CLAIM CONSTRUCTION CHART

Motorola's '814 Patent (Vaglica)		
Claim	**Claim No.**	**Court's Construction**
from said first subset to said second subset; and		
control means for disabling said mode switch means from switching to said second subset of said instructions.	10[C]	Corresponding structure: logic for latching the state of the BKPT signal.
13. A data processor comprising:	13[A]	Term not identified as needing construction.
execution means for sequentially executing a plurality of instructions, said execution means having a first mode in which instructions of a first subset are executed and a second mode in which instructions of a second subset are executed;	13[B]	CPU (11) including IR PIPE 51, execution unit 52, sequencer 53, and microcode 54.
communication means for providing said plurality of instructions to said execution means, said communication means operating in a master mode while providing instructions of said first subset and in a slave mode while providing instructions of said second subset, said communication means is coupled to a first plurality of pins and to a second plurality of pins, **said communication means uses the first plurality of pins while providing instructions of the first subset and uses the second plurality of pins while providing instructions of the second subset, each of the second plurality of pins is either not used or is used only for development support functions while the communication means is providing instructions of the first subset;**	13[C]	IMB (12); Bus Controller (40/50); Background Mode Serial Logic (45); Serial Interface (55).

APPENDIX A: CLAIM CONSTRUCTION CHART

Motorola's '814 Patent (Vaglica)		
Claim	**Claim No.**	**Court's Construction**
mode switch means for switching between said first mode and said second mode and for preventing said communication means from operating in said slave mode while said execution means is executing instructions of said first subset.	13[D]	Structure responsive to BKPT (in bus controller 50), to background instruction, or to double bus faults; logic that asserts FREEZE signal; instruction to resume normal mode; logic for latching the state of the BKPT signal.
14. A data processor according to claim 13 wherein said communication means further comprises:	14[A]	Term not identified as needing construction.
controller means for operating a parallel communication bus as a bus master; and	14[B]	35 U.S.C. 112(6) governs: The corresponding structure is the same as for 1[B] (i.e. bus controller 40 in Fig. 3 and 50 in Fig. 4).
a slave-only serial communication interface	14[C]	Term not identified as needing construction.
17. A data processor according to claim 13 wherein:	17[A]	Term not identified as needing construction
said mode switch means is responsive to an externally-provided signal to switch from said first mode to said second mode	17[B]	35 U.S.C. § 112 ¶ 6 does not apply. No construction necessary.
20. A data processor according to claim 13 further comprising	20[A]	Term not identified as needing construction.
control means for disabling said mode switch means from switching to said second mode of operation.	20[B]	Logic for latching the state of the BKPT signal.